WLCSP

Wafer Level Chip Scale Package

Wafer Level Chip Scale Packaging (WLCSP) is a Fan-in wafer level package (FIWLP) that provides signi□cant package footprint reductions, lower cost, improved electrical performance, and a relatively simpler construction over conventional wirebond or interposer packaging technologies.

in WLP services that enable higher current densities & increased reliability

- Repassivation, Redistribution, Bumping and IPD layer options available
- Full turnkey wafer bumping & Flip Chip-in-Package assembly capability

Features

- WLCSP body sizes quali□ed up to 6x6mm
- Ball count ranges depending on pitch size and up to 300mm
- Die services available for 8”-12” wafers
- In-house thin □lm on wafer processing & bumping
- Full service wafer bumping with Polyimide or PBO dielectric options for wafer repassivation, redistribution and IPD layers
- Bumps formed by printed paste, electroplate or ball drop solder bump technologies
- Minimum available □ip chip bump pitch of 150 m
- Large bump (220-500 m) processing at 0.35mm pitch & greater for Flip Chip-on-Board & WLCSP applications
- For larger pitch applications, either printed paste bumping or mechanical ball drop available
- Eutectic and Pb-free solder
- Copper under bump metallization (UBM) & redistribution layers (RDL) available
- Wafer level IPD & thick copper (8-12 m) conductors available
- Under□lling of substrate mounted bumped die may or may not be required depending on customer’s speci□c application & reliability requirements
- Under□lling by overmolding is feasible
- Low cure temperature polymers available
- Flexible bare die processing
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