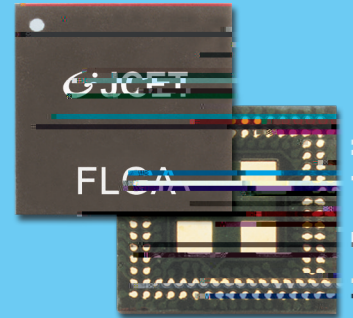


Highlights

- Array molded, cost effective, space-saving packaging solution
- Available in 2.45mm (LFLGA), 1.20mm (TFLGA), 1.00mm (VFLGA) and 0.80mm (WFLGA) maximum thickness
- Thinner than FBGA
- Exposed thermal/mechanical lands available
- Laminate substrate based enabling 2 and 4 layers of routing flexibility



Features

- Low profile
- Flexible body sizes range from 4 x 4mm to 13 x 13mm
- Flip chip and discrete passive options (SiP)
- Minimum 0.50mm pitch (array and peripheral land pads)
- Flexible land pattern arrangement
- Pb-free and halogen-free compatible materials available
- JEDEC standard compliant

Applications

- Handheld devices
- Wireless RF
- Analog
- ASIC
- Memory
- Simple PLDs

Description

Fine Pitch Land Grid Array (FLGA) is a laminate substrate based package with plastic overmolded encapsulation. Unlike a standard FBGA, second level interconnect is achieved on the LGA by connecting “lands” on the package directly onto the PCB through solder reflow.

The elimination of solder balls brings better electrical performance and lower package profile without using the more expensive thinner BT core material. It also offers the flexibility of land pattern arrangement in the form of signal lands or heat spreader/ground pads to suit the thermal and electrical requirements of various devices.

The FLGA package’s reduced outline and thickness make it an ideal advanced technology packaging solution for high performance and/or portable applications. Our FLGA is available in a broad range of JEDEC standard body sizes including LFLGA (<2.45mm), TFLGA (<1.20mm), VFLGA (<1.00mm) and WFLGA (<0.80mm) package thickness.

Specifications

Die Thickness
Gold Wire
Pd/Cu Wire
Ag Wire
Mold Cap Thickness
Marking
Packing Options

Reliability

Moisture Sensitivity Level JEDEC Level 2A, 260°C Reflow
Temperature Cycling Condition C (–65°C to 150°C), 1000 cycles

High Temperature Storage 150°C, 1000 hrs
Pressure Cooker Test 121°C, 100% RH/2 atm, 168 hrs
Temperature/Humidity Test 85°C/85% RH, 1000 hrs
Unbiased HAST 130°C/85% RH/2 atm, 96 hrs

Thermal Performance θ_{ja} (°C/W)

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Performance θ_{ja} (C/W)
VFLGA	9 x 9 (4L)	112	4.1 x 4.1	36.1

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance

Cross Sections

FBGA